

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Amendment, filed 7/15/08, with respect to the rejection(s) of claim(s) 1-18 and 20 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Objections

2. Claim 1 is objected to because of the following informalities: on line 20, please change "a local signal" to -- the local signal --.
3. Claim 5 is objected to because of the following informalities: (a) on line 17, please change "the decimation filter" to -- a first decimation filter --. (b) on line 21, please change "the decimation filter" to -- a second decimation filter --. (c) on line 24, please change "a local signal" to -- the local signal --.
4. Claim 16 is objected to because of the following informalities: on line 11, please delete "and inverting" and add -- inverted and non-inverted --.
- Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 5, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view of Yasuda (US 6,181,740), further in view of Poklemba (US 5,696,796).

a) Regarding to claim 1, Chalmers disclose a digital down-converter for converting a frequency of a signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediate frequency (IF), to a detection frequency for a detection process, comprising:

a first mixer (106 in Fig. 1) for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the signal by a real signal (since the current application is direct to local oscillator DDS 202, Chalmers's local oscillator has the same functionality as the current application) ; and

a second mixer for converting the frequency of the first IF signal having only wanted components outputted to a second IF signal of the detection frequency (126 and output of 132,134 as shown in Fig. 1).

Chalmers disclose all the subject matters described above except for the specific teaching of (1) a decimation filter and (2) a digital signal down converter; a first selector and a second selector.

However, (1) Yasuda., in the same field of endeavor, discloses a receiver system comprises an analog decimation filter to suppress the signal which may turn out to be aliasing noise (105 in Fig. 3; Col 2, L40-47). Therefore, it is obvious to one of ordinary skill in art to implement the analog decimation filter of Yasuada after the first mixer of

Chalmers (106 in Fig. 1), and before the second mixer (126, 132 and 134). The signals are converted to digital signals after the second mixer in the receiver system of Chalmers. By doing so, remove unwanted or undesired signal in a radio receiver system.

(2) Moreover, Poklemba, disclose a digital down converting system comprises A/D converter (204) output to a digital down converter (as shown in Fig. 6). And a first selector for cyclically selecting and inverting signals and outputting the second IF signal as a complex signal equivalent to a signal produced by multiplying the second IF signal by cosine wave values of a local signal (206 and 208); and a second selector for cyclically selecting and inverting signals and outputting the second IF signal as a complex signal equivalent to a signal produced by multiplying the second IF signal by sine wave values of a local signal (206 and 210; Col 5, L51-59; Though Poklemba does not explicitly describe two selectors, Poklemba sequentially selects from cosine (+1,0,-1,0) and sine (0,+Q,0,-Q) values (Fig. 4 and 6). The current application also sequentially selects from values of 1,0,-1,0 and 0,1,0,-1. Therefore, Poklemba implicitly teaches two selectors.). Therefore, it is obvious to one of ordinary skill in art to implement the sampling method of Poklemba in the receiver system of Chalmers and Yasuda. By doing so, provide no phase imbalance, I/Q crosstalk, and DC offsets in a digital downconverting system. In addition, the quadrature translation can be implemented through multiplication by cosines and sines whose sample values are (+1,0,-1,0) and (0,-1,0,-1), respectively (Col 1, L55-59). Therefore, reduce circuitry complexity.

b) Regarding to claims 5 and 16, Chalmers disclose a receiver comprising:

a digital down-converter including a first mixer (106 in Fig. 1) for converting a frequency of the received signal, sampled with a radio frequency (RF) or an intermediate frequency (IF), to a frequency of a first IF signal by multiplying the signal by a real signal (120), and a second mixer (112 in Fig. 1) for converting the first IF signal converted by the first mixer to a second IF signal of the detection frequency for a detection process (126 and output of 132,134 as shown in Fig. 1).

an RF unit (received signal as shown in Fig. 1) for receiving an input signal and providing the received signal to the digital down-converter for frequency conversion.

Chalmers disclose all the subject matters described above except for the specific teaching of the RF unit output to a third mixer; a filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter, from an output of the third mixer; an analog-to-digital converter for sampling an output of the filter with a radio frequency or an intermediate frequency and providing the sampled signal to the digital down-converter; and a first selector and a second selector in the second mixer.

However, (1) Yasuda., in the same field of endeavor, discloses a receiver system comprises an analog decimation filter to suppress the signal which may turn out to be aliasing noise (105 in Fig. 3; Col 2, L40-47). Therefore, it is obvious to one of ordinary skill in art to implement the analog decimation filter of Yasuda at the output of block 116 (Fig. 1) of Chalmers. This way, the quadrature converter of Chalmers comprises two decimation filters, wherein the first decimation filter is operated at In-phase signal

(I), and the second decimation filter is operated at the quadrature signal (Q). By doing so, remove unwanted or undesired signal in a radio receiver system.

Moreover, (2) Poklemba, disclose a digital down converting system comprises IF signal output to an anti-aliasing filter (202), A/D converter (204), and a digital down converter (as shown in Fig. 6). It is well known and common knowledge to implement a mixer for RF signal converting to IF signal. Thus, a third mixer (input to filter 202) is inherently taught. In addition, Poklemba disclose a first selector for cyclically selecting and inverting signals and outputting the second IF signal as a complex signal equivalent to a signal produced by multiplying the second IF signal by cosine wave values of a local signal (206 and 208); and a second selector for cyclically selecting and inverting signals and outputting the second IF signal as a complex signal equivalent to a signal produced by multiplying the second IF signal by sine wave values of a local signal (206 and 210; Col 5, L51-59). Though Poklemba does not explicitly describe two selectors, Poklemba sequentially selects from cosine (+1,0,-1,0) and sine (0,+Q,0,-Q) values (Fig. 4 and 6). The current application also sequentially selects from values of 1,0,-1,0 and 0,1,0,-1. Therefore, Poklemba implicitly teaches two selectors. Therefore, it is obvious to one of ordinary skill in art to implement the sampling method of Poklemba in the receiver system of Chalmers. By doing so, provide no phase imbalance, I/Q crosstalk, and DC offsets in a digital downconverting system. In addition, the quadrature translation can be implemented through multiplication by cosines and sines whose sample values are (+1,0,-1,0) and (0,-1,0,-1), respectively (Col 1, L55-59). Therefore, reduce circuitry complexity.

5. Claims 2-15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view of Yasuda (US 6,181,740), further in view of Poklemba (US 5,696,796), and in further view of Ostman (US 6,061,385).

a) Regarding to claims 2, 6, and 17, Chalmers, Yasuda, and Poklemba disclose all of the subject matter described above except for the specific teaching of a frequency of the first IF signal is $\frac{1}{4}$ a sampling frequency.

Ostman, in same field of endeavor, teaches a received frequency modulated signal as shown in Fig. 1, where the intermediated frequency is a quarter of the sampling frequency (Col 4, L28-36).

To avoid complexity and extreme power consumption of the circuitry a well known method is to select the intermediate frequency to be a quarter of the sampling frequency (Ostman, Col 4, L28-35). Therefore, it is obvious to one of ordinary skill in the art to implement quarter sampling method taught by Ostman in the frequency down conversion system by Chalmers. By doing so, provide simpler digital down converter design and more desirable result. Additionally, reduce power consumption, reduce cost, and simplify communication system design.

b) Regarding to claims 3, 7, 11, and 18, Chalmers discloses further comprising an automatic gain control (AGC) amplifier (110 in Fig. 1) for amplifying of the output of the first mixer and inputting the amplified output to the cosine part and the sine part of the second mixer, and

wherein the first and second selectors are connected to the output of the AGC (Chalmers in view of Poklemba).

- c) Regarding to claims 4 and 9, Chalmers discloses the digital down-converter, wherein the second mixer further comprises a multiplier for multiplying the output of the decimation filter by a certain ratio of a sampling frequency and a decoding means for decoding the multiplied signal through the multiplier (as shown in Fig. 1).
- d) Regarding claim 8, wherein the second mixer of the digital down-converter is constructed in a polyphase structure comprised of a decimation filter and a quadrature converter, and wherein the first and second selectors are connected to the output of the decimation filter (Yasuda's decimation filter 105 in Fig. 3 is implemented at the output of 116 in Fig.1 of Chalmers. Chalmers's quadrature converter (132,134,126,128 in Fig. 1) is replaced with Poklemba's quadrature converter (206,208,210 in Fig. 6).).
- e) Regarding to claim 10, the digital down-converter further comprises: wherein the first and second selectors are connected to the output of the decimation filter (Yasuda, and Poklemba).
- f) Regarding to claims 12 and 13, Poklemba disclose wherein the first selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value 1, outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0' (106 and 108 in Fig. 4; Col 5, L51-59).
- g) Regarding to claims 14 and 15, Poklemba disclose wherein the second selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value 1, outputs a multiplication

result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0' (106 and 108 in Fig. 4; Col 5, L51-59).

Allowable Subject Matter

7. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Puente whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner, Art Unit 2611

October 23, 2008

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611